REMARKS

Claims 1-36 remain pending in the application.

35 U.S.C. § 103(a) Rejections:

Claims 1 and 2 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen ("On Chip Decoupling Capacitor Optimization for Higher Performance VLSI Design" IEEE 1998) in vew view of Peil, U.S. Patent 4,806,937 and in further view of Hanf, U.S. Patent 6,438,462. Claims 3, 6, 7, 11, and 12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and Hanf, and in further view of Brown, U.S. Patent 5,960,207 and Chan, U.S. Patent 6,466,898. Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanve, Brown, and Chan, and in further view of Skelton, U.S. Patent 6,147,478 and Smith ("Packaging and Power Distribution Design Considerations for Sun Microsystems Desktop Workstation", IEEE 1997). Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanf, Brown, Chan, and in further view of Schutz, U.S. Patent 5,444,298. Claims 13 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Brown, Smith, and Chan. Claims 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and in further view of Brown, Smith, Chan, and Chun ("Investigation of Voltage Regulation Stability of Static Synchronous Compensator in Power System", IEEE January 2000). Claims 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and Hanf and in further view of Brown, Chan, and Smith. Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and Hanf and in further view of Brown, Chan, Smith, and O'Sullivan ("Developing Decoupling Methodology with SPICE for Multilayered Printed Circuit Boards", IEEE 1998). Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and Hanf and in further view of Brown, Chan, Smith, and Schutz. Claims 21-24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil and Hanf and in further view of Brown, Chan, Smith, and Skelton. Claims 25 and 26 were rejected under 35 U.S.C. §

103(a) as being unpatentable over Chen in view of Peil, Hanf, and O'Sullivan. Claims 27, 30, 31, 35 and 36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanf, and O'Sullivan and in further view of Brown and Chan. Claims 28 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanf, and O'Sullivan and in further view of Brown, Chan, and Chun. Claim 32 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanf, and O'Sullivan and in further view of Brown, Chan, Skelton, and Smith. Claims 33 and 34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Peil, Hanf, and O'Sullivan and in further view of Brown, Chan, and Schutz. Applicant respectfully traverses these rejections.

The cited references, taken singly or in combination, do not teach all of the elements of the independent claims. Chen teaches on-chip power bus modeling and switching noise analysis for high performance circuit design, and the methodology to optimize the placement of on-chip decoupling capacitors. The switching noise is analyzed at both the package level and the chip level. An equivalent circuit which consists of time-varying resistors, loading capacitors, and decoupling capacitors, is used to simulate the switching activities of functional blocks. Both the resistive and inductive voltage drops on the power bus are modeled to identify the hot spots on the chips and ΔV across the chip. Based on the noise analysis results, a decoupling capacitor insertion algorithm is proposed to determine the amount of decoupling capacitance needed to keep the power supply voltage within specification, and optimize the final size and location of on-chip decoupling capacitors.

Hanf teaches a semiconductor circuit for an electronic unit having at least one microcontroller which comprises at least one voltage regulator for providing, from a first supply voltage, at least one second supply voltage for the microcontroller and for circuits of the unit which cooperate with the microcontroller. The circuit further comprises, in monolithic form, a transceiver unit having transmitting and receiving device for coupling a microcontroller to the two-wire bus. This monolithic construction may additionally comprise watchdog functions, various wake-up functions and an interface via which a

serial data exchange with the at least one microcontroller is possible. Furthermore, it may have an apparatus for determining, throughout the network, bus subscribers having reference-ground potential faults and for quantifying such faults.

Peil teaches a system which relates to the distribution of power and control commands to a plurality of pulsed T/R modules coupled to the antenna elements of a phased array radar. The power distribution system includes a large number of small capacitors, at least one per module, a lesser number of large capacitors, at least one at each end of each row, and bus bars dimensioned for a very small r.f. impedance for supplying peak power in a timely manner to the modules from the large capacitors. Each row has four large (1KW) dc power supplies for providing the average power. The power conditioning elements within the modules are of reduced bulk while achieving "droop" free operation. The control commands are carried by lower current capacity runs on a layer laminated to the bus bar. Connectors attached to the laminated bus bar and indexed at the module positions provide high power and control commands. The arrangement permits automated testing of the connections and is of high reliability.

O'Sullivan teaches a SPICE model employed to examine the impedance of a typical power bus on a multilayer PCB. This impedance is calculated at numerous points (or nodes) around the board with respect to the noise sources and as a result the choice and quantity of decoupling capacitors as well as placement information and the resulting impact on the power supply impedance is evaluated.

In contrast, Applicant teaches a system and method for determining decoupling components for a power distribution system having a voltage regulator module. Independent claim 1 recites, in pertinent part:

> "A system for determining decoupling components for a power distribution system, said power distribution system including a voltage regulator module, the system comprising ... a computer system configured to ...

simulate a voltage regulator circuit using a mathematical model of said voltage regulator circuit, wherein simulating said voltage regulator circuit includes:
simulating a voltage with a voltage source model;
simulating ramping up or ramping down of current in said voltage regulator circuit with a model of a slew inductor; and
simulating effects of output inductance on said voltage regulator circuit with a model of an output inductor" (Emphasis added)

Independent claim 25 recites a similar combination of features. Independent claim 13 recitees "simulating the operation of said voltage regulator circuit using a model of said voltage regulator circuit."

The cited references, taken singly or in combination, do not teach or suggest all of these features. In particular, Applicant can find no teaching or suggestion in any of the cited references of simulating a voltage regulator circuit, simulating ramping up or ramping down of current in the voltage regulator circuit with a model of a slew inductor, or simulating the effects of output inductance on the voltage regulator circuit.

In the office action, the Examiner contends that Peil teaches simulating a voltage regulator circuit at column 12, line 65 to column 13, line 15, column 13, lines 32-48, and Figures 6, 7A, and 7B. Applicant respectfully disagrees and submits that the sections of Peil cited by the Examiner are directed towards a power distribution system for a phased array radar. Column 12, lines 33-36 of Piel states that "The operation of the power distribution system from the large one kilowatt supplies (4) to the individual T/R module (32) loads may best be explained by reference to FIGS. 7A and 7B." Peil also states, in column 13, lines 4-9 that "The simulated performance assumes the simplified equivalent circuit representation illustrated in FIG. 7A. In the equivalent circuit diagram, the one kilowatt power supply (4) coupled to one end of the bus bar (3) is represented by the 80 ampere generator at the left extremity of the figure" (Emphasis added). Furthermore, as is well known to those skilled in the art, a voltage regulator circuit is designed to maintain a substantially constant output voltage. In Figure 7B of Peil, the voltage vs.

time performance shows a significant fluctuation in the voltage on bus bar 3. Applicant submits that this performance is not consistent with a voltage regulator. In light of these remarks, Applicant submits that Peil does not teach the simulation of a voltage regulator circuit as recited in the independent claims in the sections cited by the Examiner, and cannot find these teaching elsewhere in Peil.

With regard to the Hanf reference, the Examiner contends that Hanf teaches simulating the ramping up or ramping down of current in a voltage regulator circuit, and cites Hanf at column 17, line 51, to column 18, line 29, which refers to the operations of slew rate controller 170, one of which is included in each of function blocks 110, 120, and 130 (see Figure 4 of Hanf). None of these function blocks is described as a voltage regulator by Hanf. In function block 110, slew rate controller 170.1 is shown in Figure 4 of Hanf as coupled wake-up identification block. Function block 120 (which includes slew rate controller 170.2) is described by Hanf as a receiving means (col. 17, line 21). Function block 130 (which includes slew rate controller 170.3) is described by Hanf as a transmitting means (col. 17, line 22). Applicant can find no teaching or suggestion of simulating the ramping up or ramping down of current in a voltage regulator circuit in anywhere in Hanf, including the sections cited by the Examiner.

In addition, with regard to the rejection of claim 25, the Examiner asserts that O'Sullivan teaching the simulating of a voltage regulator circuit. Applicant respectfully disagrees. Applicant can find no teaching or suggestion of the simulation of a voltage regulator circuit anywhere in O'Sullivan, including in the sections cited by the Examiner.

For at least the reasons, Applicant submits that the cited references, taken singly or in combination, do not teach all of the elements of the independent claim. Accordingly, removal of the 35 U.S.C. § 103(a) rejections against each of these claims is respectfully requested. With respect to the remaining 35 U.S.C. § 103(a) rejections, Applicant notes that each of the claims subject to these rejections is dependent upon on of the independent claims discussed above, and thus each of these claims is believed allowable for at least the same reasons.

CONCLUSION

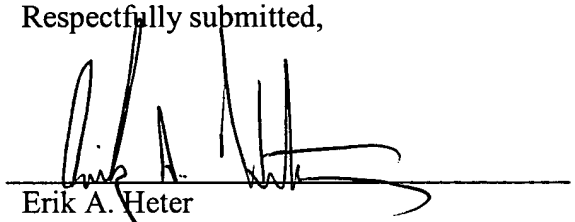
Applicants submit the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-33801/BNK.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

Respectfully submitted,



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Date: 11/17/04